**Layout Guidelines for 31-0001 Rev 2**

1. Reference files
   1. Mechanical drawing: 31-0001-2\_Mech.PDF
   2. Schematic: 31-0001-2\_Schematic.pdf
   3. Netlist: 31-0002-2\_NetList.asc
2. This board requires a ground planes on both the top and bottom for the purposes of shielding low frequency (<1KHz) interference.
3. This should be a 4-layer board. All nets other than “GND\_SIGNAL” should be routed on the inner layers as much a practical.
4. No trace on the board carries more than 1mA, so the trace width can be small.
5. There are no impedance requirements as this is a low frequency application.
6. “31-0001-2\_Mech.PDF” shows the approximate position of the silkscreen identifiers for the 8 electrode pins. How these identifiers map to the actual netlist is shown on the schematic and below.

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| **Electrode Designator** | **Silkscreen Identifier** | **Net Name** |
| P1 | A1V1 | N01127 |
| P2 | A1V2 | N01115 |
| P3 | A1V3 | N01103 |
| P4 | A1V4 | N01091 |
| P5 | A2V1 | N01139 |
| P6 | A2V2 | N01151 |
| P7 | A2V3 | N01163 |
| P8 | A2V4 | N01175 |